1. (amended) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a bit line that is a component of the DRAM and a connection layer that is located in a common layer with the bit line and which is used to electrically connect a lower electrode of the capacitor element and another semiconductor element;

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(b) simultaneously forming a storage node of the cell capacitor and the lower electrode of the capacitor element;

(c) simultaneously forming a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

(d) simultaneously forming a cell plate of the cell capacitor and an upper electrode of the capacitor element.

2. (amended) A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(e) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (e) is carried out simultaneously with the step (d), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

Please add new claims 17-26 as follows:

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5. ~~17.~~ (new) A method for manufacturing a semiconductor device according to claim 1, further comprising forming a first resistance element and a second resistance element in the analog element region, the first resistance element and the second resistance element each being formed in a region comprising a semiconductor, wherein forming the first resistance element includes performing a number of ion-implantations of impurity that is greater than a number of

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ion-implantations performed for forming the second resistance element, so that a resistance value of the first resistance element is lower than that of the second resistance element.

6. ~~18.~~ (new) A method for manufacturing a semiconductor device according to claim 5 ~~17~~, wherein the semiconductor comprises silicon.

7. ~~19.~~ (new) A method for manufacturing a semiconductor device according to claim 1, further comprising forming a first resistance element and a second resistance element in the analog element region, the first resistance element and the second resistance element each being formed in a region comprising a semiconductor, wherein forming the first resistance element includes diffusing an impurity into the region comprising a semiconductor, so that the first resistance element has a resistance value that is lower than that of the second resistance element.

A3 cont.

8. ~~20.~~ (new) A method for manufacturing a semiconductor device according to claim 7 ~~19~~, wherein the semiconductor comprises silicon.

9. ~~21.~~ (new) A method for manufacturing a semiconductor device according to claim 1, further comprising forming a first resistance element and a second resistance element in the analog element region, the first resistance element and the second resistance element each being formed in a region comprising polysilicon, wherein the first resistance element formed to include a silicide layer and the first resistance element is formed to have a resistance value that is lower than that of the second resistance element.

12. ~~22.~~ (new) A method for manufacturing a semiconductor device according to claim 11 ~~16~~, wherein the third conducting layer comprises a semiconductor.

13. ~~23.~~ (new) A method for manufacturing a semiconductor device according to claim 11 ~~16~~, wherein the third conducting layer comprises polysilicon.

14. ~~24.~~ (new) A method for manufacturing a semiconductor device according to claim 13 ~~23~~, further comprising forming the first resistance element to include a silicide layer.

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15.
11 ~~25.~~ (new) A method for manufacturing a semiconductor device according to claim ~~16~~, wherein the third conducting layer comprises polysilicon, and further comprising forming the first resistance element by a method including implanting an impurity into a region of the polysilicon.

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16.
11 ~~26.~~ (new) A method for manufacturing a semiconductor device according to claim ~~16~~, wherein the third conducting layer comprises polysilicon, and further comprising forming the first resistance element and the second resistance element by a method including implanting a greater amount of an impurity into the first resistance element than into the second resistance element.--

REMARKS

Applicant has amended claims 1-2, canceled claims 5-14 without prejudice, and added new claims 17-26. Claims 1-4 and 15-26 are currently pending. Reexamination and reconsideration are respectfully requested.

Claims 1 and 2 have been amended for clarity. Claims 5-14 have been canceled without prejudice as non-elected claims.

In the specification, applicant has amended the paragraph starting on page 1, line 6, to insert the serial numbers as requested by the Examiner.

Claims 1-4 were rejected under 35 U.S.C. 112, second paragraph. The rejection is respectfully traversed.

The Examiner stated that "in claim 1, step (b), 'the lower electrode' in indefinite. Applicant does not agree with the Examiner because element (a) of claim 1 recites in part ". . . a lower electrode of the capacitor element . . ." However, for clarity, as noted above, element (b) of claim 1 was amended to recite in part ". . . the lower electrode of the capacitor element . . ."

The Examiner stated that for claims 2-4, "it is unclear how the resistance value be adjusted by ion-implantation of impurity in the resistance element if it is of metal? Or how could the silicide is formed if the resistance element is not of polysilicon?" Applicant does not understand the Examiner's rejection relating to claims 2-4, specifically, applicant is unsure of which terms the Examiner objects to as being indefinite. For example, claim 2 does not specify a particular material to be implanted into and applicant is unsure if the Examiner is objecting to the

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